REMARKS

By this response, claims 1, 2, 10, and 17 have been amended. Accordingly, claims 1 through 17 are active in this application and reconsideration of all active claims is respectfully requested.

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Claim Rejection 35 U.S.C. § 112

.The Examiner rejected claims 1-6, 8-12, 14, and 16-17 under 35 U.S.C. § 112, first paragraph.

The Examiner indicated in reference to claims 1 & 2: the phrase "wherein said second insulator thinkness is greater than the first insulator and said second insulator having a second value of said given parameter that is different from said first value" is unclear. The disclosure describes only second insulator having a second value of said given parameter which is selected from the group consisting of density, thickness and insulative value but not together. There is no support for the second insulator having a different parameter including together thickness and density or insulative value. The Applicants have amended the claims to clearly indicate that the second insulator has a second value which is selected from a group in accordance with the specification.

Claims 3-6 and 8-9 were rejected because each includes the limitations of independent claim 1. By this amendment the limitations of independent claims which should be allowable under 35 U.S.C. § 112, first paragraph.

Claim 10 was rejected because the phrase "a first device having a diode..." is not supported by disclosure. The disclosure only describes the first device having antifuse. Claim 10 has been amended to indicate that the first device is an antifuse to overcome the rejection based on 35 U.S.C. § 112.

Claims 11-12, 14, & 16 were rejected because each includes the limitations of independent

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claim 10. By this amendment to overcome the rejection based on the limitation of claim 10 should now be allowable along with dependent claims 11-12, 14 & 16.

Claim 17 was rejected because the phrase "a first integrated circuit element comprising a diode.." is not supported by disclosure. The disclosure only describes the first integrated circuit element comprising an antifuse. Claim 17 has been amended to indicate that the first device is an antifuse to overcome the rejection based on 35 U.S.C. § 112, first paragraph.

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Claim Rejection 35 U.S.C. § 102

The Examiner rejected claim 1 under 35 U.S.C. § 102(b) as being anticipated by Chen, et al. (US5,656,534).

The Examiner indicated regarding claim 1, Chen et al. teach a programmable element, comprising (Fig 3): a first device (10) on a substrate (18) having a first electrode (36') and a first insulator (28) disposed between the substrate and said first electrode, said first insulator having a first value of a given parameter; a second device (12) on a substrate (18) having a second electrode (36") and a second insulator (26) disposed between the substrate and said second electrode, said second insulator having a second value of said given parameter that is different from said first value (Col.3, lines 60-65).

It should be noted that Chen is not addressing the same problem that is being addressed by the subject application in that Chen teaches ESD protection (device 10) of an antifuse (device 12) wherein the dielectric thickness of the protection circuit in 10 is less than the dielectric thickness of the antifuse, device 12. The devices (10 and 12) are separated by an isolation feature, 20. This ordering of elements is diametrically opposite to that in subject invention. Referring to the figures 1B and 6 of the present invention, device 16A is the Anti-Fuse, and device 16B provides gain such that a high impedance anti-fuse can be read using a conventional latch. These devices SHARE a common diffusion node, and does not require separation by an isolation feature. This is one of the novel aspects of the present invention. The antifuse 16A has different characteristics than the gain device 16B. Thus, this invention is quite different than Chen, based on the physical structure of the antifuse versus external devices. In addition, Chen does NOT

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teach the use of a gain device to assist in the reading of a high impedance (Post programmed) anti-fuse. Chen specifically references patents 4,823,181 and 4,899,205, which discuss LOW impedance antifuse elements. It is understood that a LOW impedance anti-fuse is sometimes considered a desirable result, but there exists a stistical HIGH impedance tail on greater than 1% of the population of programmed anti-fuses rendering these antifuses unreliable. In fact, they cannot guarantee a properly sensed, or latched result. Hence the present invention is directed to structure that can reliably handle the high impedance of a post programmed Anti-Fuse. Chen does NOT address or contemplate this problem. In fact, since Chen's anti-fuse dielectric is THICKER than the surrounding parallel device dielectrics, one would question Chen's ability to program such dielectrics as they are in parallel with the protection circuitry. This creates a layer of complexity that we do not have to solve. For example Chen's ESD device 10 has to be disabled during anti-fuse (device 12) programming, as device 10 by Chen's description would program, or in this case undergo damage prior to the anti-fuse. Thus, Chen would have to hold node 14 at the programming potential of node 36. This technique (although it requires another wiring interconnect) will work assuming node 10 did not undergo an ESD damaging event. If node 10 was damaged through an ESD event, then there would be a low impedance path between nodes 16 –>36–>14 or vice versa pending the programming polarity, thus making it impossible to program device 12. Chen basically has two MOS capacitors, with device 10 (ESD protection device) having a gate that is shared with device 12 (Anti-fuse) and a separate diffusion 14, and another diffusion (16) for the anti-fuse, hence three terminals. But, in our invention, the three electrodes create a MOSFET device, clearly not the same as Chen's structure. Further, with regard to claim 13 it should be noted that Chen does not teach a gain device as his device 10 is a capacitor versus wherein our invention the gain device is a MOSFET. Also, the thickn ss of

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Chen's Anti-fuse oxide as contrasted with surrounding devices is quite different than our invention.

Chen (5,656,534) teaches a first ESD diode (10) having a first insulator thickness that is thinner than a second Antifuse(12). The ESD device (10) is for the purpose of protecting the antifuse 12, during semiconductor processing. Two layers of polysilicon conductors are required to connect the devices (10) and (12).

It should be noted also that in our invention, we use MOSfets not DIODES, that have their gates connected with one level of polysilicon. Two levels are not required. As shown in figure 1C, our devices have a shared diffusion node, (21). If Chen shares his diffusion node, his antifuse diode device would be shorted to the ESD protection device, rendering the antifuse device unuseable. Chen uses the sedond device (i.e., the ESD device (1)) to protect the antifuse device. As such, during processing the ESD device is EXPECTED to conduct prior to the antifuse device, conducting energy away from the antifuse device. This teaches away from our invention.

Furthermore, in our embodiment, the second device is used to PROGRAM the antifuse device, without itself conducting energy away from the antifuse device. Thus in our case the second device is used to supply energy to the antifuse in a controlled manner. In this way, where the first device is the fuse having a "weak" insulator so that when programmed it will decrease in resistivity and not effect the second device or the second insulator which will not program.

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Accordingly, Claim 1 has been amended to include all the innovative features described above which should now overcome the rejection based on 35 U.S.C. § 102(b). Accordingly, it is respectfully submitted that Claim 1 is allowable under 35 U.S.C. § 102(b) and should be passed to issue.

ALLOWABLE SUBJECT MATTER

It is noted with appreciation that the Examiner allowed claims 7, 13, and 15.

The Examiner indicated that Claims 10-12, 14, 16, and 17 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, first paragraph, set forth in this Office Action.

By this response claims 10 and 17 have been amended to overcome the rejection(s) under 35 U.S.C. 112, first paragraph, set forth in this Office Action. Accordingly, it is respectfully submitted that claims 10-12, 14, 16 and 17 are now allowable.

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Conclusion

Based on the foregoing, it is respectfully submitted that all the claims active in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
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